



Fig. 1

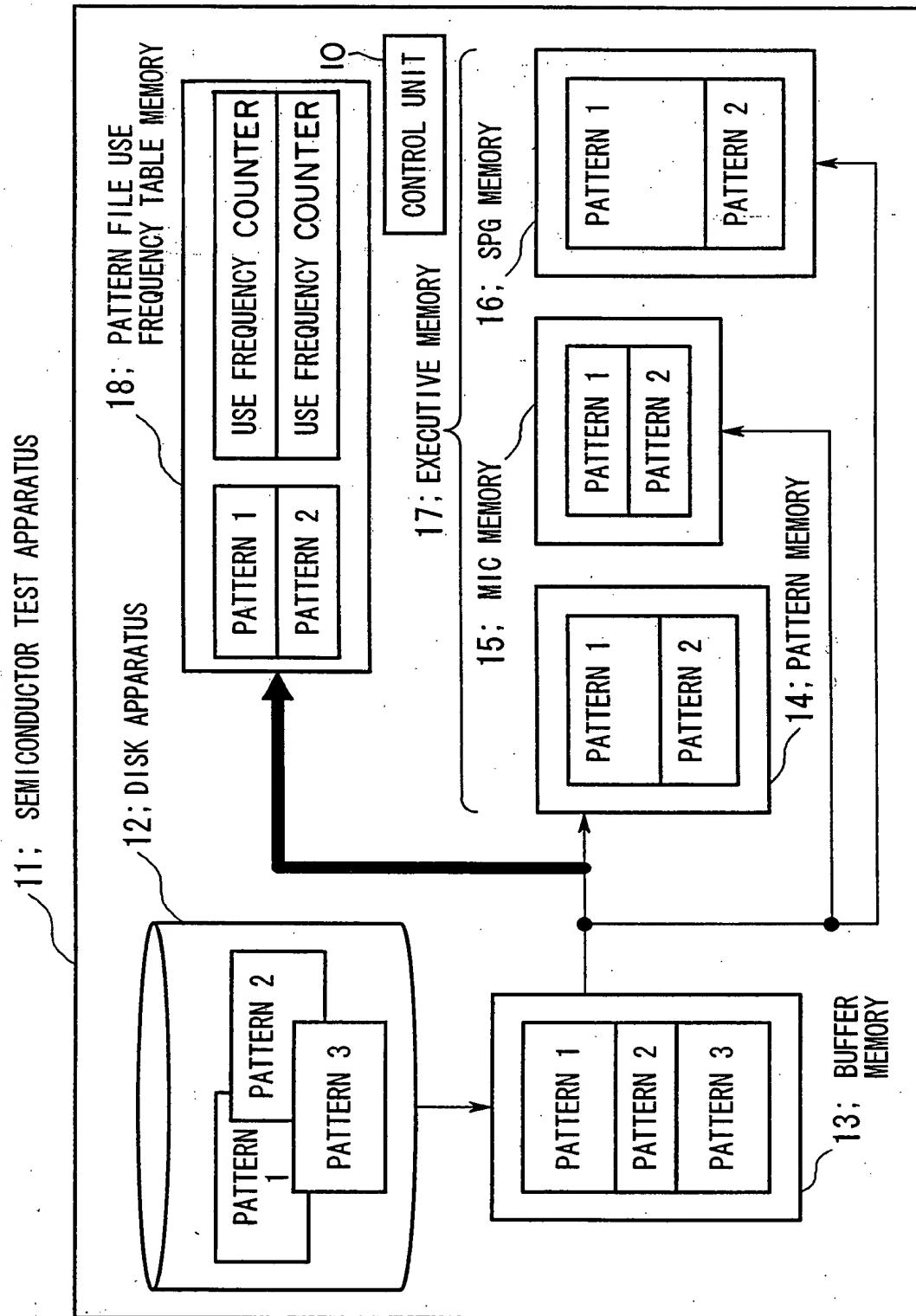




Fig. 4 (PRIOR ART)

41: SEMICONDUCTOR TEST APPARATUS

42; DISK APPARATUS

40

CONTROL UNIT

EXECUTIVE MEMORY

45: MIC MEMORY 46: SPG MEMORY

PATTERN 1	PATTERN 2
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PATTERN 1
PATTERN 2
PATTERN 3

43; BUFFER MEMORY

42; DISK APPARATUS

40; CONTROL UNIT

43; BUFFER MEMORY

44; PATTERN MEMORY

45; MIC MEMORY

46; EXECUTIVE MEMORY

46; SPG MEMORY

The diagram illustrates the memory hierarchy and data flow in a disk apparatus. It features five main memory components arranged vertically:

- 40; CONTROL UNIT**: A rectangular box at the top.
- 46; EXECUTIVE MEMORY**: A large rectangular box containing a sub-diagram. The sub-diagram shows a vertical stack of three rectangular boxes labeled **PATTERN 1**, **PATTERN 2**, and **PATTERN 3**. Arrows point from the **40** box to the **46** box, and from the **46** box to the **45** box.
- 45; MIC MEMORY**: A rectangular box containing a sub-diagram. The sub-diagram shows a vertical stack of two rectangular boxes labeled **PATTERN 1** and **PATTERN 2**. Arrows point from the **46** box to the **45** box, and from the **45** box to the **44** box.
- 44; PATTERN MEMORY**: A rectangular box containing a sub-diagram. The sub-diagram shows a vertical stack of two rectangular boxes labeled **PATTERN 1** and **PATTERN 2**. Arrows point from the **45** box to the **44** box, and from the **44** box to the **43** box.
- 43; BUFFER MEMORY**: A rectangular box at the bottom containing a sub-diagram. The sub-diagram shows a vertical stack of three rectangular boxes labeled **PATTERN 1**, **PATTERN 2**, and **PATTERN 3**. Arrows point from the **44** box to the **43** box, and from the **43** box to the **42** box.

Arrows indicate the flow of data from the **40** box through the **46**, **45**, and **44** boxes to the **43** box, and then back to the **42** box. The **46** box also has a direct connection to the **45** box.



Fig. 5

(PRIOR ART)

